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SF-7739

B. E. IV (Sem. VIII) (ECC) Examination

May / June – 2011

Advance Microprocessor : Elective - I

Time : **3** Hours] [Total Marks : **100**

Instructions :

(1)

નીચે દર્શાવેલ ☛ નિશાનીવાળી વિગતો ઉત્તરવહી પર અવશ્ય લખવી.
Fillup strictly the details of ☛ signs on your answer book.

Name of the Examination :

☛ **B. E. 4 (Sem. 8) (ECC)**

Name of the Subject :

☛ **Advance Microprocessor : Elective - 1**

☛Subject Code No. : **7 7 3 9** ☛Section No. (1, 2,.....) : **Nil**

Seat No. :

Student's Signature

(2) Attempt all questions.
(3) Figures to the right indicate full marks.
(4) Assume suitable data whenever necessary and mention clearly your assumptions.
(5) Use of non programmable scientific calculators is allowed.

1 (a) Answer following questions :

(i) What is the function of FSC in 8086 ? **2**

(ii) Explain the following pin function in 8086 when it operates in Maximum mode, S_0, S_1, S_2. **2**

(iii) The 8087 internally stores all the numbers in which format ? Why ? **2**

(iv) What is the function of Block transfer mode in DMA CONTROLLER ? 8237 ? **2**

(v) State the different methods of data communication. **1**

(vi) What is the baud rate of RS-423 ? **1**

(b) (i) Write a program to find the resonant frequency of an LC tank circuit using 8087 and 8086 instructions and directives. **6**

(ii) Explain the daisy chaining priority scheme in loosely coupled Multiprocessor system. **4**

2 (i) Draw and explain timing diagram for maximum mode bus requests and grants. **4**

(ii) Explain the cascaded mode of 8259 with connection diagram. **6**

(iii) Explain the function of the following pins of 8251 IC. **5**
(a) DTR
(b) RTS
(c) CTS
(d) DSR
(e) SYNDET/BRDET

OR

2 (i) Explain in detail the function of PCI bus. **6**
(ii) Explain in brief how bus controller generates the control signals in 8086 maximum mode. **6**
(iii) Explain following instructions : **3**
(a) FSAVE
(b) FRSTOR.

3 Attempt any **three** : **15**
(i) Explain following instructions :
(a) FXRCT
(b) FPREM
(c) FNOP.
(ii) Explain 6845 CRT controller screen memory/character generator with CPU.
(iii) Draw internal architecture of 8251 and explain briefly.
(iv) Briefly explain the function of following signals generated by 8272 floppy disk controller :
(a) DRQ
(b) DACK
(c) LCT/DIR
(d) FR/STP
(e) MFM.
(v) Explain Asynchronous mode of 8251.

4 (a) Answer the followings : **10**
(i) The Pentium Pro can execute_____ simultaneous instructions.
(ii) When 80386 operated in protected mode memory segment size range from _____ to _____.
(iii) Using _____ the Pentium Pro is able to look ahead as many as 30 instructions.
(iv) At any given time the 80386 has _____ active segments.
(v) The 386 keeps track of the 32 most recently used page frames in the _____.
(vi) Using 386 debug registers_____ different breakpoint addresses can be set.

(vii) The P6 processors can execute _____ instructions per cycle.

(viii) For a memory interface to work properly, the access time provided by the processor must be _____ the access time of the memory chip.

(ix) The _____ addressing mode is used with complex data structures.

(x) To determine if a memory location is stored in the cache the _____ bits are compared with the high order memory address bits.

(b) Which of the following 80X86 microprocessors have more than one instruction decoder ? **4**

(a) 8086
(b) 8088
(c) 80386
(d) 80386SX
(e) 80486
(f) 80486SX
(g) Pentium
(h) 80186

(c) Calculate the size of segment for one descriptor with G=1 and segment size limit bits are all 1. State significance of granularity bit. **6**

5 (a) With the help of functional block diagram explain the various blocks of Pentium processor and their functions in brief. **8**

(b) Compare and contrast Superpipelined and Superscalar architecture. **7**

OR

5 (a) With the help of diagram explain the concept of cache memory and explain the 80486 cache memory organization considering all aspects. **8**

(b) What do you mean by protection in multitasking environment ? Explain protection mechanism in 80386. **7**

6 Attempt any **three** : **15**

(a) Calculate the total no. of bits of SRAM storage required to implement the Pentium cache.

(b) Reorder the instruction below to allow optimum execution by the Pentium's dual pipelines.

```
ADD AL, BL
DEC AL
INC CL
MOV BL, DL
```

(c) Design an 80486 8-bit input and output port both mapped to port FFFCH. Write a program to read data from the input port and output this data to the output port.

(d) Explain the operation of ENTER/LEAVE instructions with suitable example.

(e) Write a far procedure 'read2' to read a character from keyboard and reserve locations for storage of read data. The main program uses this procedure to call it 10 times and store the data as a string of characters in memory reserved by procedure. Use FAR, PUBLIC and EXTERN directives.
